In the Claims:

Claim 1 (currently amended): A method of making a flash memory cell including a substrate and a tunnel oxide layer formed on the substrate and a floating gate, the method comprising:

depositing an insulator layer ~~of~~ comprising a high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, ~~and~~ wherein the insulator layer is ~~formed around~~ in contact with vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and wherein the insulator layer ~~of high temperature oxide~~ is formed by a LPCVD process;

polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

Claims 2-3 (canceled).

Claim 4 (currently amended): The method of claim 1, wherein polishing the insulator layer includes using chemical mechanical polishing.

Claim 5 (currently amended): The method of claim 1, further comprising:

depositing a control gate layer on the ~~dielectric~~ ONO layer; and

etching the control gate layer and the ~~dielectric~~ ONO layer to form a stacked gate structure of the flash memory cell.

Claim 6 (canceled).

Claim 7 (currently amended): A method of making a flash memory cell having a substrate and a tunnel oxide layer formed on the substrate, the method comprising:

~~forming a first layer of a silicon dioxide on a floating gate of said floating gate transistor;~~

depositing a floating gate layer on the tunnel oxide layer to a first thickness;

etching the floating gate layer, to provide a floating gate;

depositing an insulator layer ~~of~~ comprising a high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate, wherein ~~such that~~ the insulator layer has a second thickness that is greater than the first thickness, wherein the insulator layer is in contact with vertical surfaces of the floating gate, and wherein the insulator layer ~~of high temperature oxide~~ is formed by a LPCVD process;

polishing the insulator layer immediately after the step of depositing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

Claim 8 (canceled).

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Claim 9 (currently amended): The method of claim 7, wherein the first thickness of the floating gate layer is between approximately 500 Å and 2000 Å, and the second thickness of the insulator layer~~, when deposited,~~ is between approximately 1000 Å and 5000 Å.

Claim 10 (currently amended): The method of claim 7, wherein polishing the insulator layer includes using chemical mechanical polishing.

Claim 11 (currently amended): The method of claim 7, further comprising:

depositing a control gate layer on the ~~dielectric~~ ONO layer; and

etching the control gate layer and the ~~dielectric~~ ONO layer to form a stacked gate structure of the flash memory cell.

Claim 12 (canceled).

Claim 13 (canceled).

Claim 14 (currently amended): The method of claim 7, wherein ~~depositing~~ the floating gate layer ~~includes depositing a~~ comprises doped polysilicon.

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Claim 15 (currently amended): The method of claim 7, wherein ~~depositing~~ the floating gate layer ~~includes depositing a~~ comprises doped amorphous silicon.

Claims 16-22 (canceled).

Claim 23 (currently amended): A method of making a flash memory cell including a substrate, a tunnel oxide layer formed on the substrate and a floating gate, the method comprising:

depositing an insulator layer ~~of~~ comprising a high quality oxide directly on the tunnel oxide layer and the floating gate, wherein the insulator layer ~~being~~ is deposited to a thickness greater than a thickness of the floating gate, ~~and~~ wherein the insulator layer ~~of high quality oxide~~ is formed on and in contact with ~~the~~ vertical surfaces ~~around~~ of the floating gate to prevent charge leaking from the floating gate, and wherein the high quality oxide is formed by a LPCVD process;

polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing an ONO layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.